PATENT ABSTRACTS OF JAPAN

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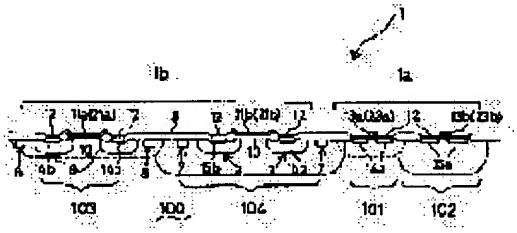
(21)Application number : **04-111330**
(22)Date of filing : **30.04.1992**

(71)Applicant : **FUJI ELECTRIC CO LTD**
(72)Inventor : **TADA HAJIME**

(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:
PURPOSE: To ensure high withstand voltage characteristics, when gate insulating films of two MIS transistor circuit parts on the same substrate are formed, in different processes.
CONSTITUTION: After a gate insulating film 10 is formed on the surface side of a single crystal silicon substrate 100, first polysilicon layer 11a, 11b are formed, and then polysilicon layers 21a, 21b are left in each gate electrode forming region of a high voltage driving circuit 1b. In this state, a gate oxide film 10 on the side of a low voltage driving circuit 1a is eliminated. After a gate oxide film 12 is formed on the side of their surface, a polysilicon layer 13 is formed on the surface side. After impurities are introduced into the polysilicon layers 13a, 13b, which are turned into a conductive state, polysilicon layers 23a, 23b are left.



LEGAL STATUS

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PATENT ABSTRACTS OF JAPAN

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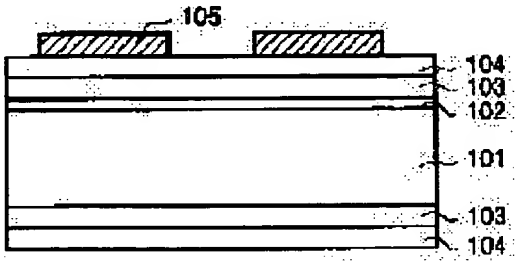
H01L 21/762

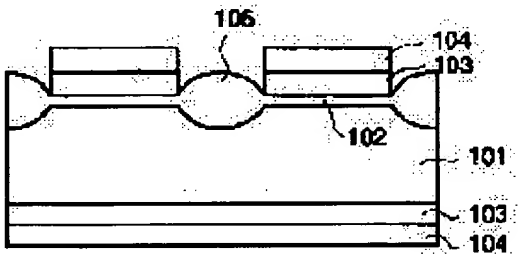
(21)Application number : **07-276063**
(22)Date of filing : **25.10.1995**

(71)Applicant : **TOSHIBA CORP**
(72)Inventor : **KOIKE HIDETOSHI**

(54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To deposit a doped silicon oxide film on a rear surface of a silicon substrate and form a gettering layer at a low temperature without increasing the number of processes by depositing a silicon thin film which serves for the gettering layer at the same time deposition of a silicon thin film to be used for an etching stopper.
SOLUTION: On a silicon substrate 101, a doped silicon thin film 103 and a silicon nitride film 104 are deposited in this order. On the silicon nitride film 104, a resist pattern 105 for forming an element isolation resion is formed. At that time, these films are deposited in the same manner on a rear surface of the silicon substrate 101. Since the doped silicon thin film 103 is brought into direct contact with the rear surface of the silicon substrate 101, it serves for a gettering layer. Nextly, the silicon nitride film 104 is etched with the doped silicon thin film 103 as an etching stopper. After that, the resist pattern 105 for forming an element isolation region is peeled off and then a silicon oxide film 106 is formed in an element isolation region.





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